

FIGURE 1
(PRIOR ART)

FIG. 2 is a block diagram of a PLL circuit.

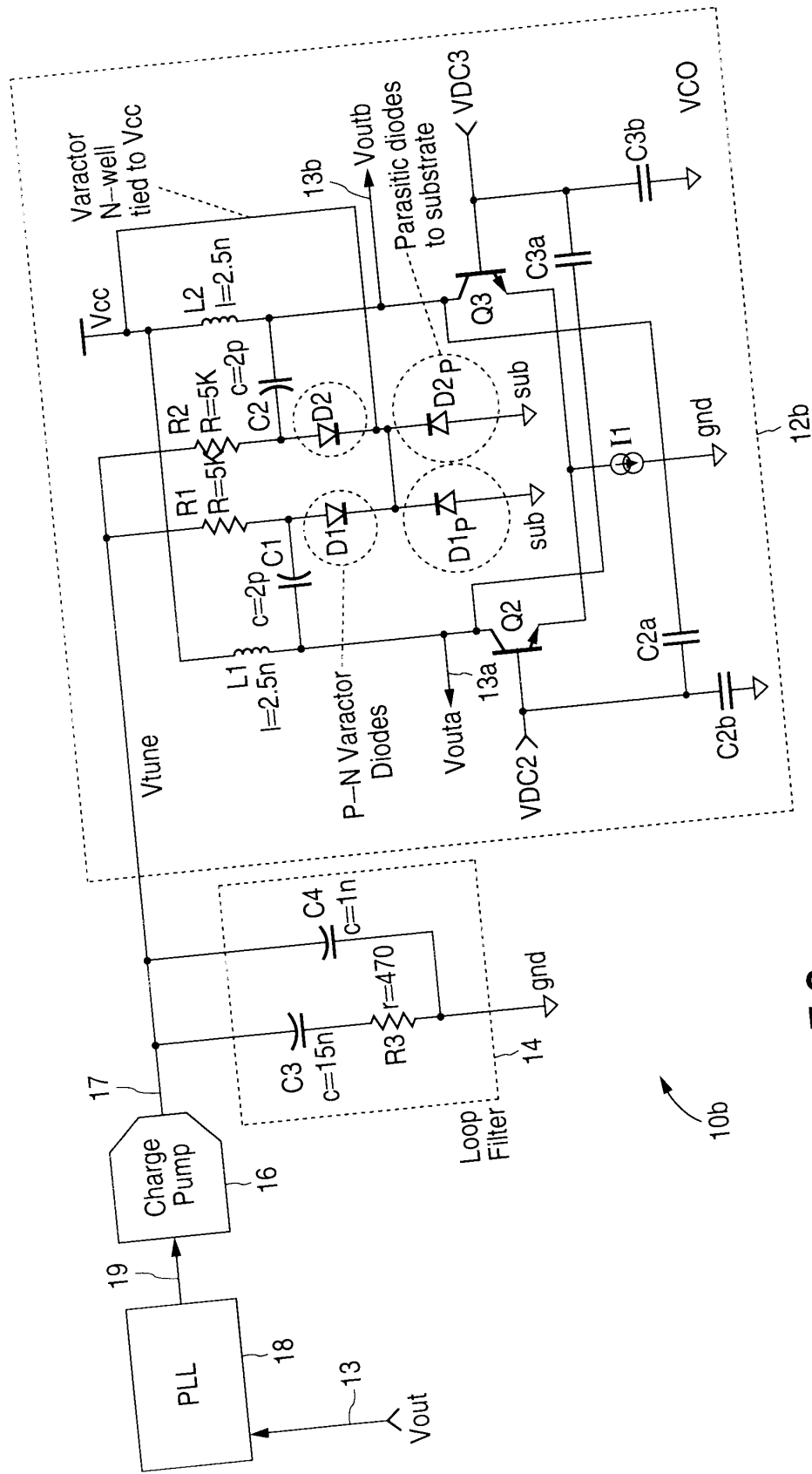


FIGURE 2
(PRIOR ART)

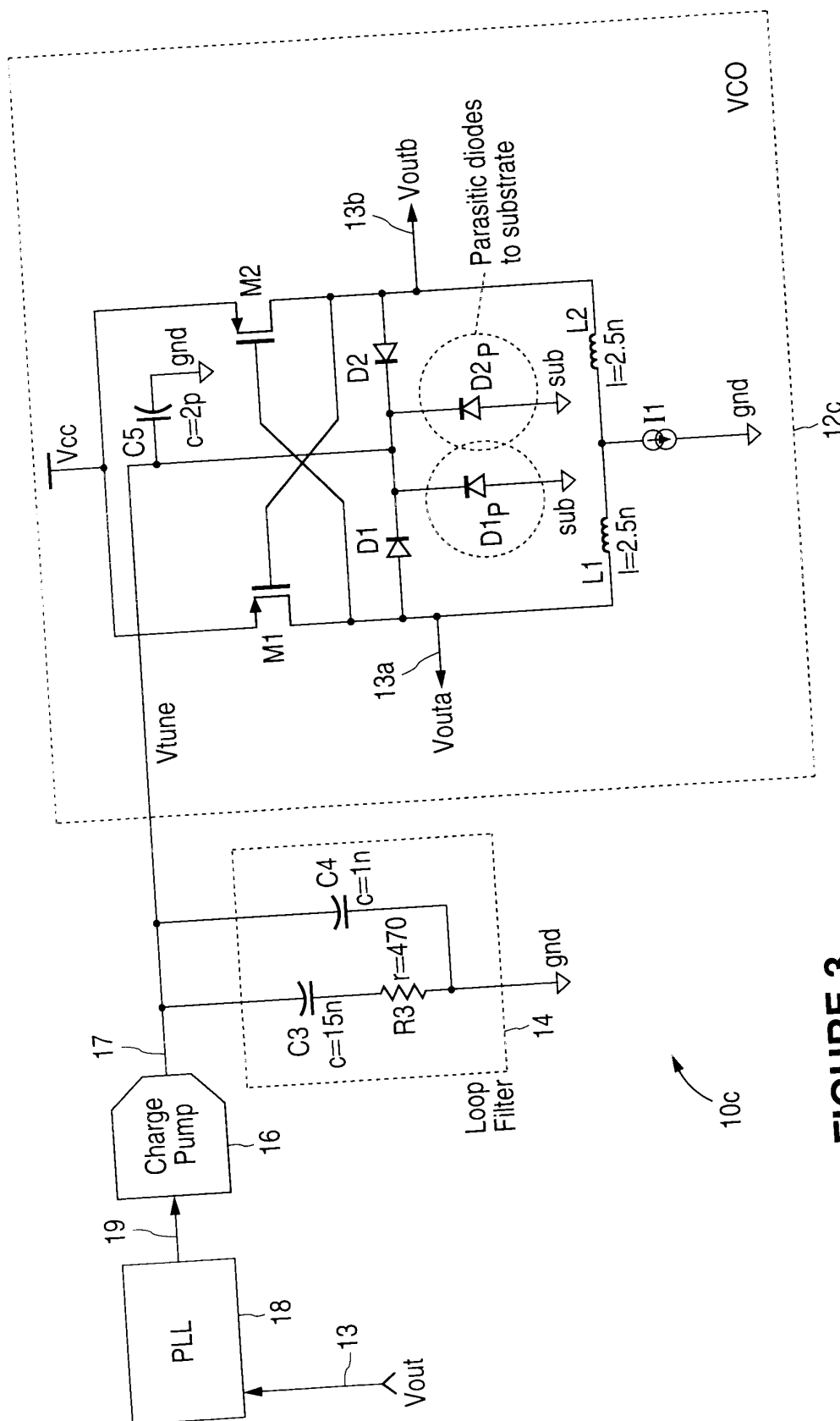


FIGURE 3
(PRIOR ART)

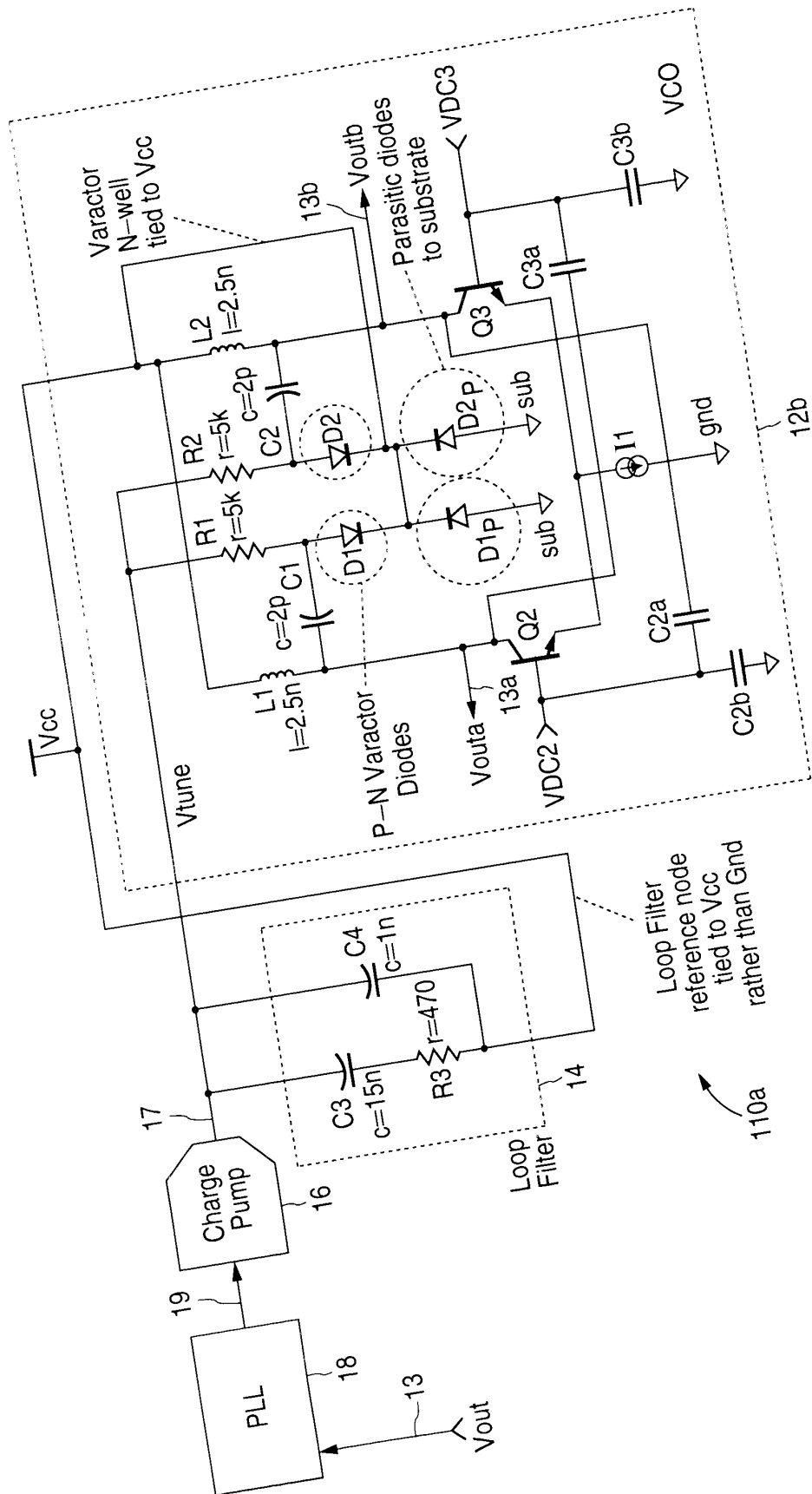


FIGURE 4

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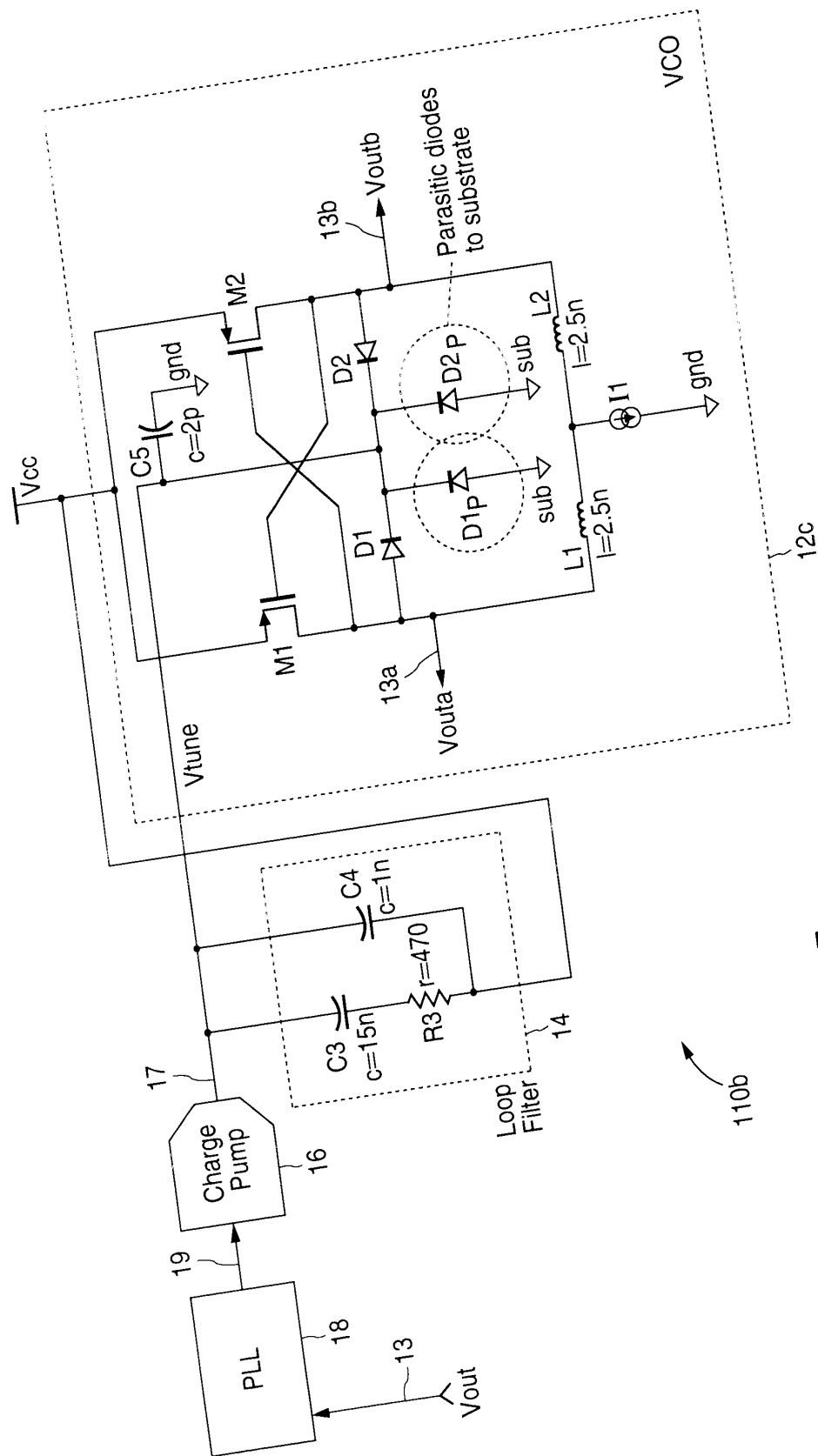


FIGURE 5

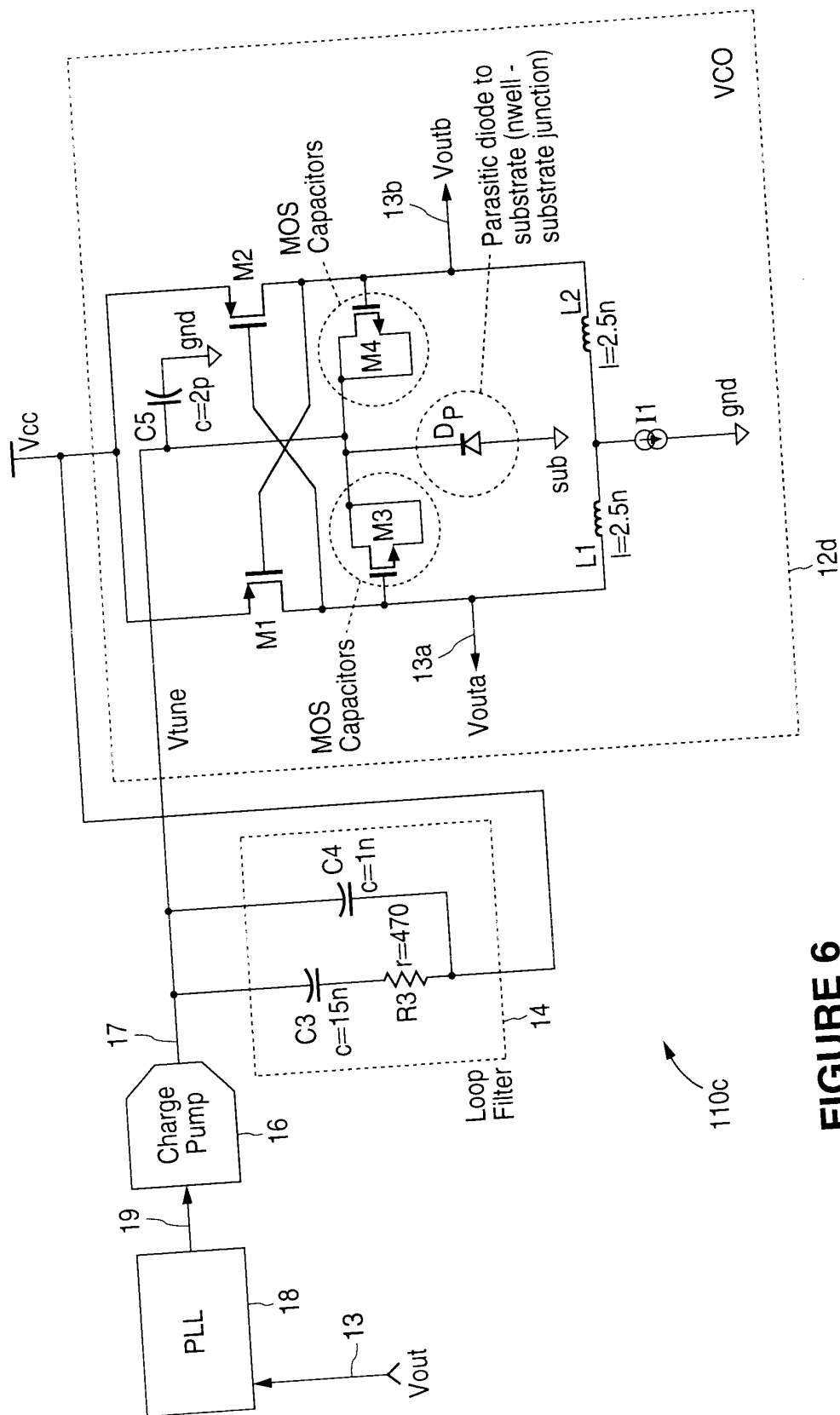
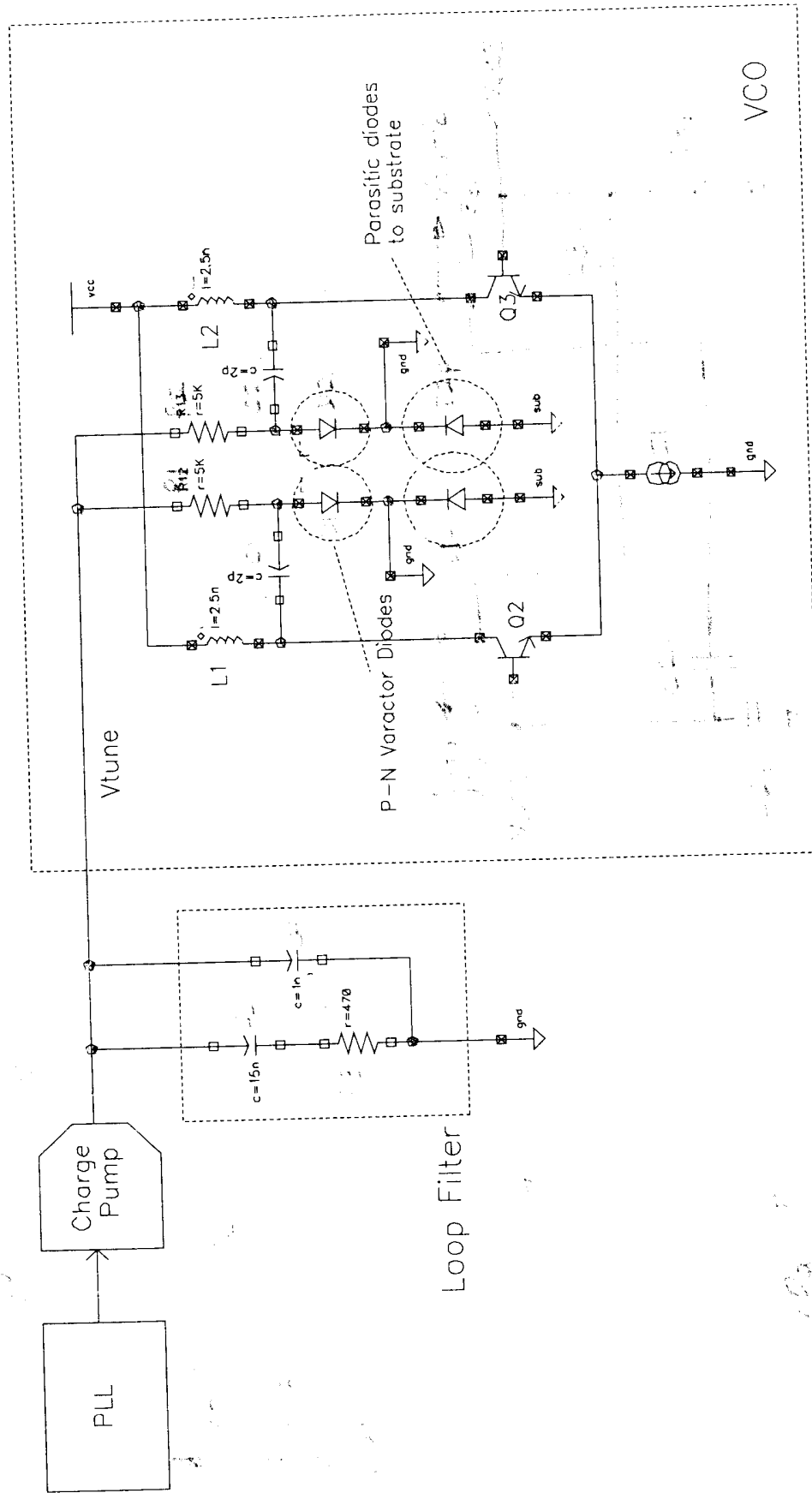
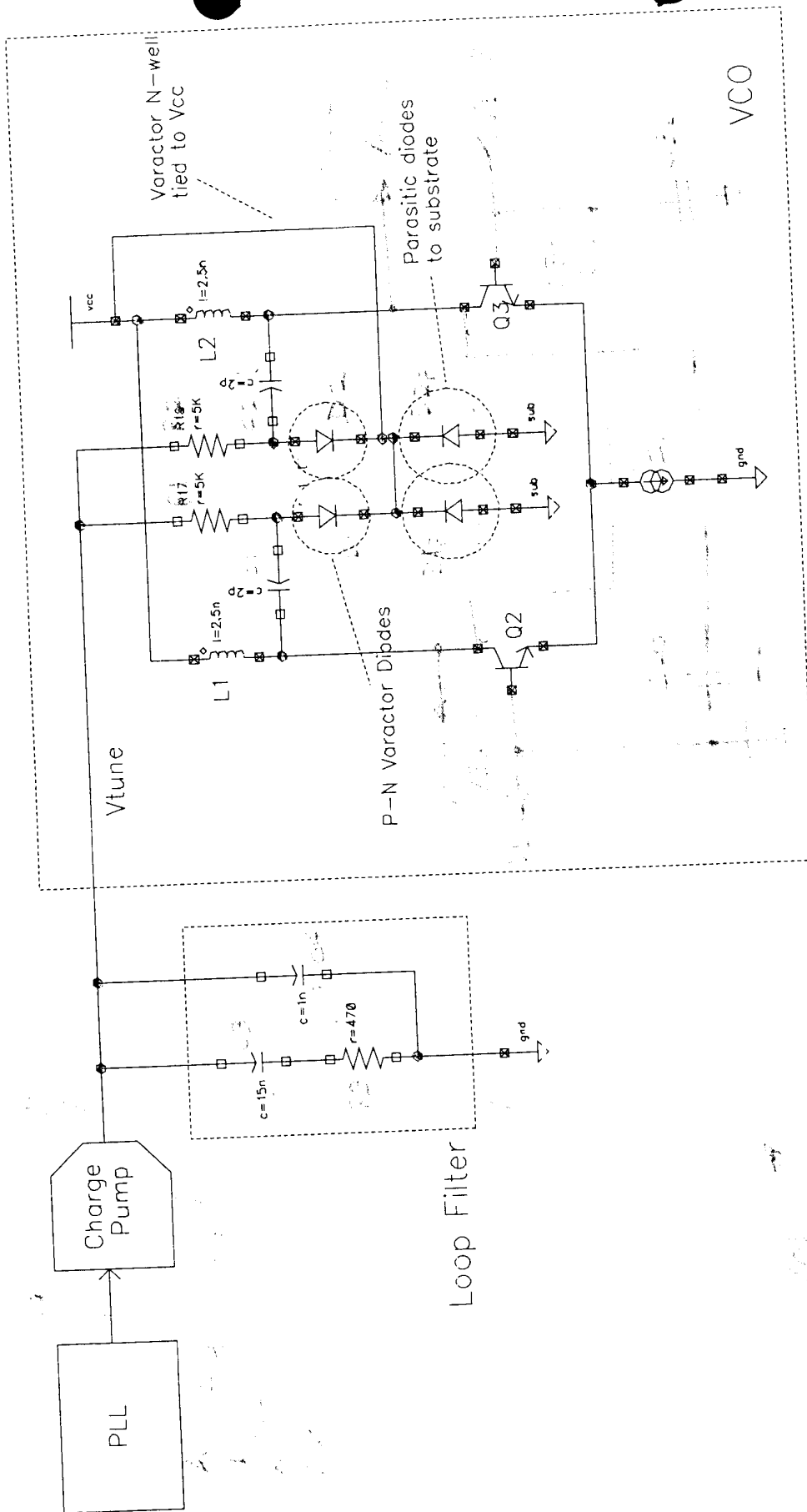


FIGURE 6





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Figure 2: PLL and VCO circuit

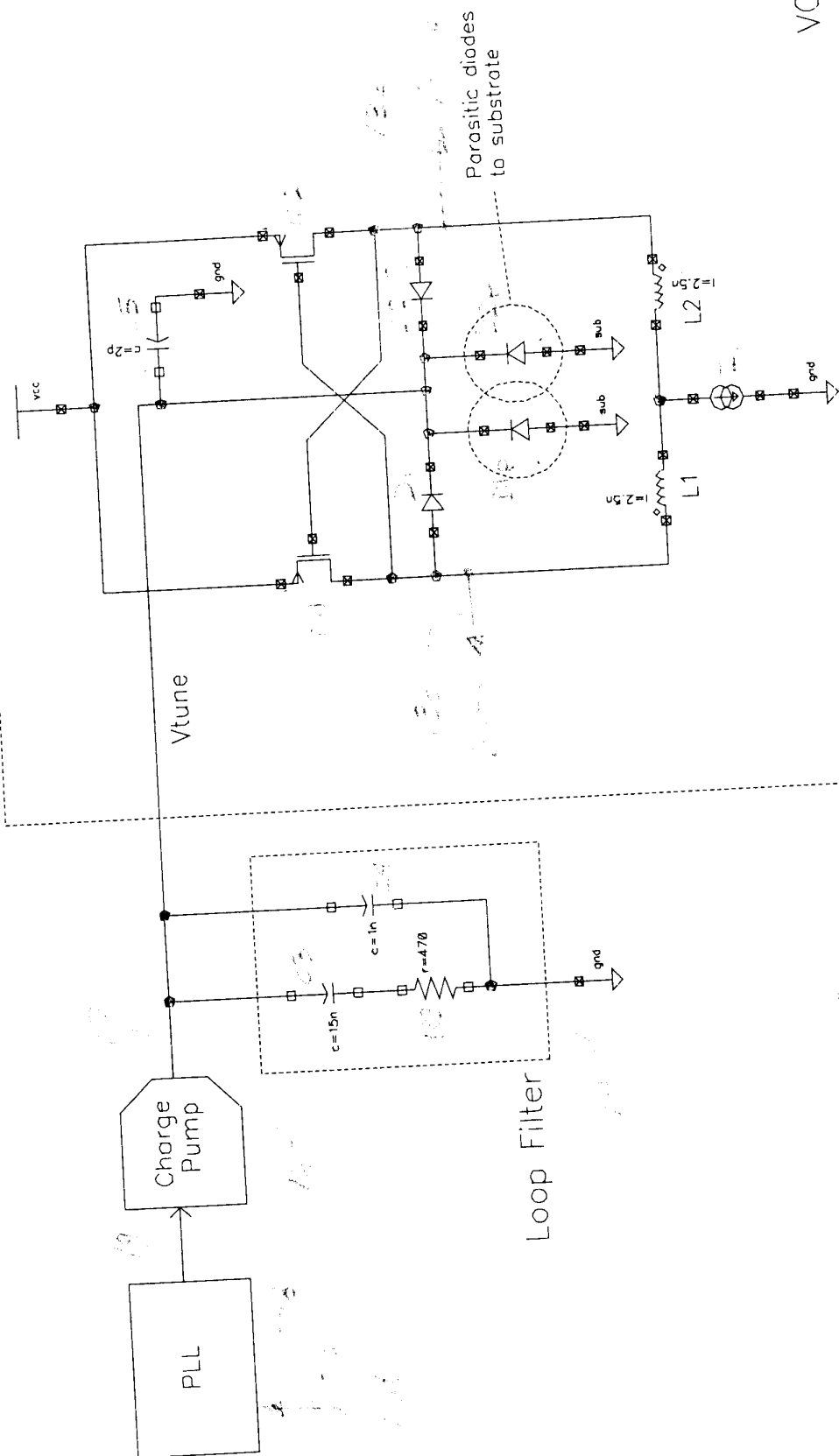
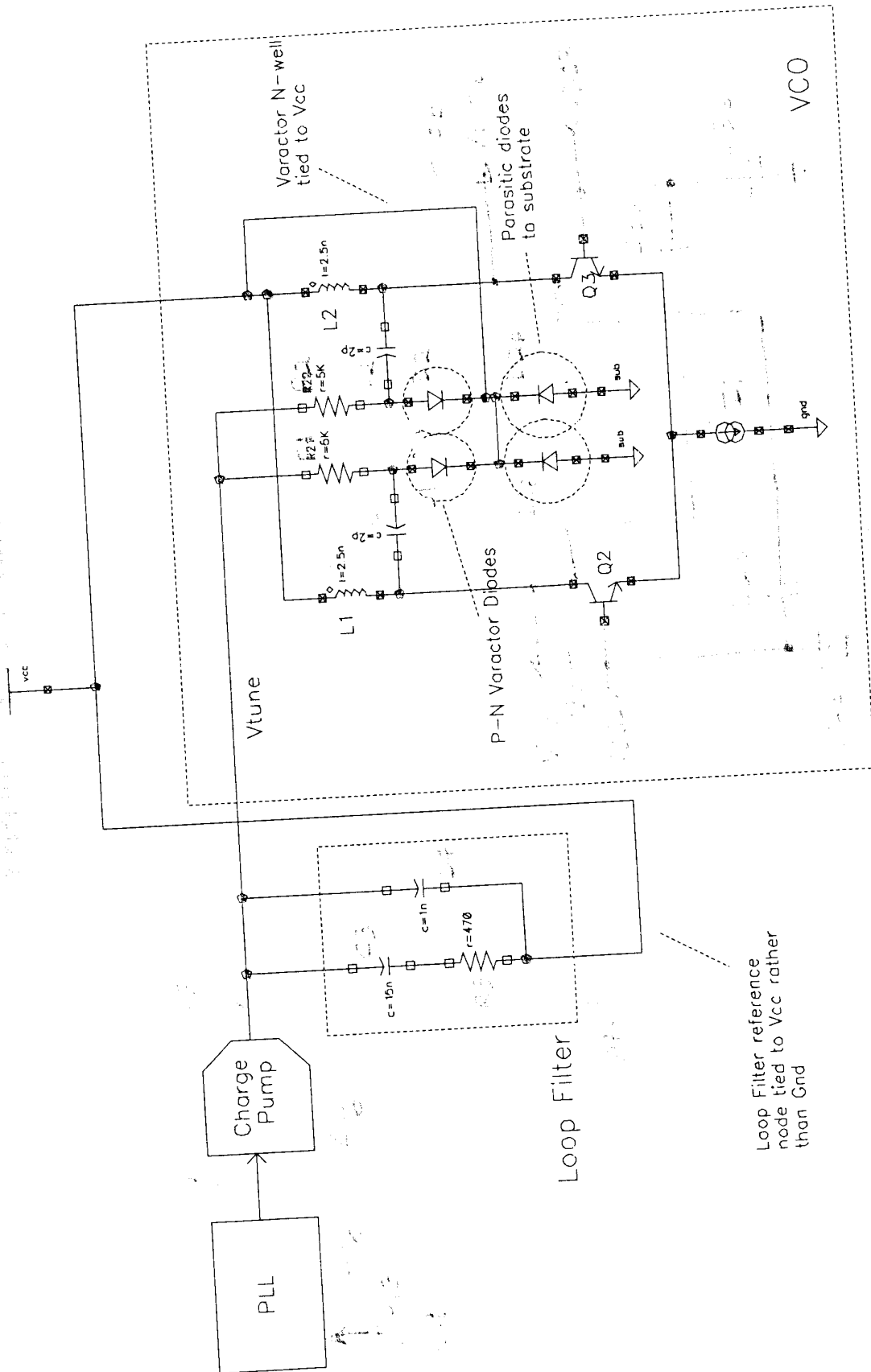


FIGURE 2
(PHASE LOCKED LOOP)

Figure 4



Loop Filter reference node tied to Vcc rather than Gnd

Figure 4

FIGURE 5

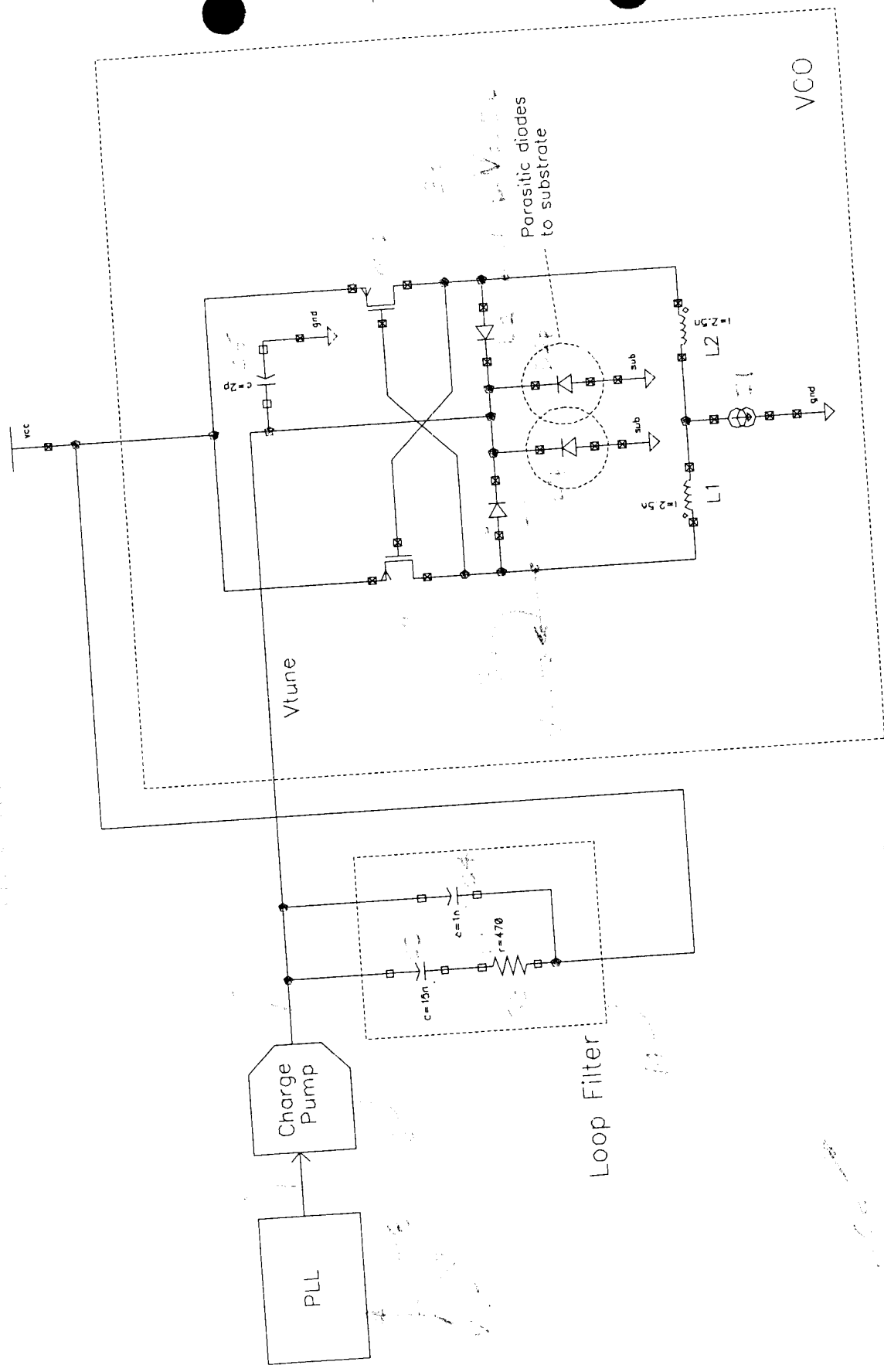


FIGURE 5

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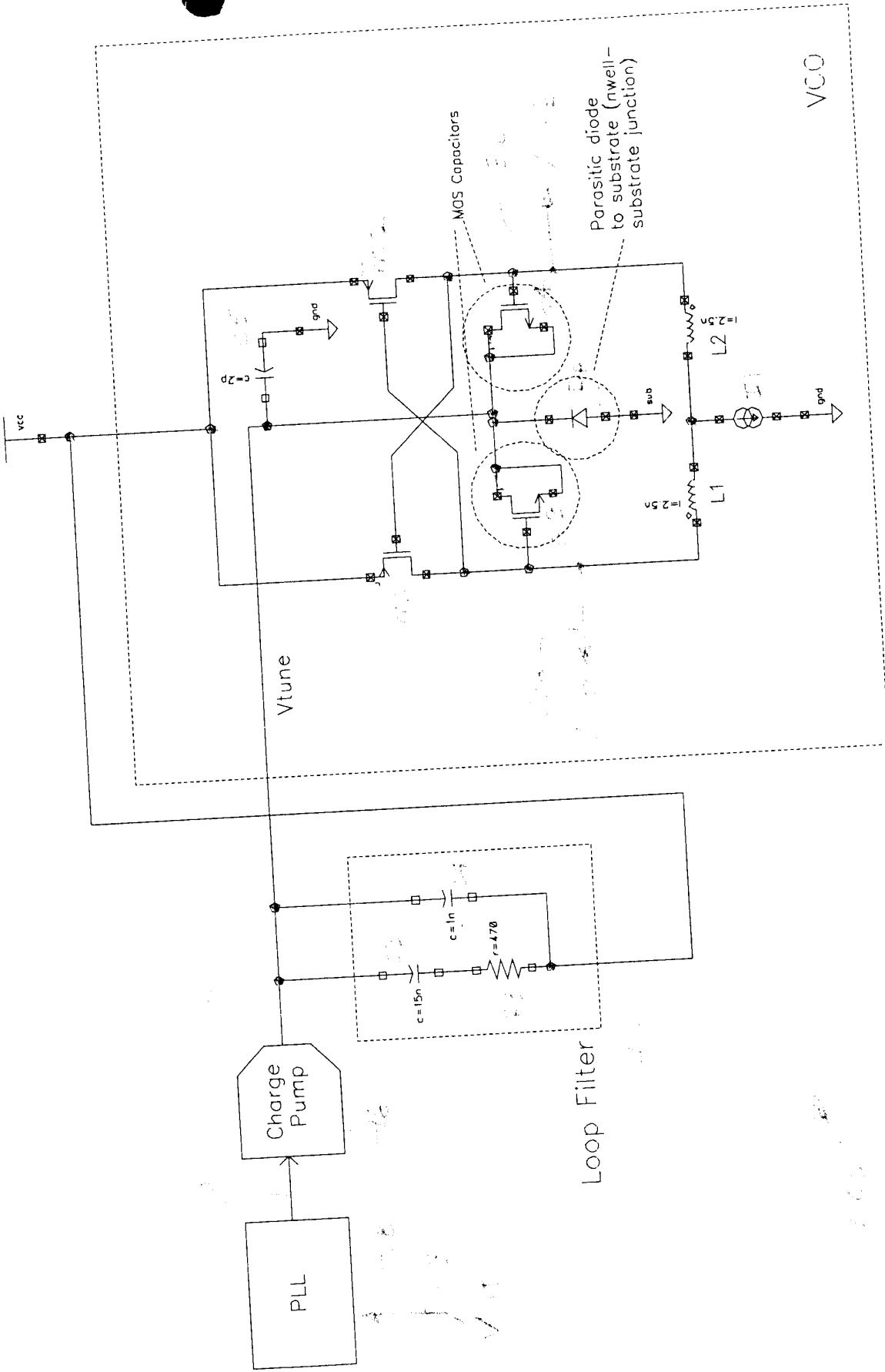


Figure 6